Paper No. 12

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte D. MITCHEL HANKS

Appeal No. 2003-1383
Application No. 09/451,414

ON BRIEF

Before FLEMING, DIXON and NAPPI, **Administrative Patent Judges.**

NAPPI, **Administrative Patent Judge.**

DECISION ON APPEAL

This is a decision on the appeal under 35 U.S.C. § 134 from the examiner's rejection of claims 1 and 2.

The Invention

The invention relates to the drive electronics used with an optical detector of data on an optical disk (see appellant's specification, page 1). The electronics for both reading and writing are combined such that a single amplifier, phase locked loop (PLL) and data detector are used (see appellant's specification, page 3).

Claim 1 is representative of the invention and reads as follows:

1. An electronic read channel for an optical disk drive, the drive adapted for reading and writing data, the channel comprising:

an amplifier, having an input and an output;

a switch, the switch coupling the input of the amplifier to a data signal when the drive is reading data, and the switch coupling the input of the amplifier to a wobble signal when the drive is writing data; and

a phased locked loop, receiving a signal derived from a signal from the output of the amplifier, the phased locked loop generating a read clock signal when the drive is reading data, and the phased locked loop generating a write clock signal when the drive is writing data.

Reference

The examiner relies upon the following reference as evidence of obviousness:

Katoh	6,088,311	July 11, 2000 (filed Jan. 9, 1998)

Rejections at Issue

Claims 1 and 2 stand rejected under 35 U.S.C. § 103 as being unpatentable over Appellant's Admitted Prior Art (AAPA) in Figure 1 in view of Katoh.

Opinion

We have carefully considered the subject matter on appeal, the rejections advanced by the examiner and the evidence of obviousness relied upon by the examiner as support for the rejections. We have, likewise, reviewed and taken into consideration, in reaching our decision, the appellant's arguments set forth in the briefs[1]

[1] This decision is based upon the Appeal Brief received November 13, 2002 (certified as being filed on November 6, 2002, in accordance with 37 C.F.R. § 1.8(a)), and the Reply Brief received February 21, 2003 (certified as being filed on February 13, 2003, in accordance with 37 C.F.R. § 1.8(a)).

along with the examiner's rationale in support of the rejection and arguments in rebuttal set forth in the examiner's answer.

With full consideration being given to the subject matter on appeal, the examiner's rejections and the arguments of appellant and examiner, for the reasons stated *infra*, we reverse the examiner's rejection of claims 1 and 2 under 35 U.S.C. § 103.

Appellant argues on page 5 of the Brief that:

> [A] combination of applicant's admitted prior art (showing two separate phase locked loops) and Katoh (showing two separate phase locked loops) does not teach or suggest one phased locked loop, generating a read clock when reading and a write clock when writing, as specified in claim 1.

The examiner asserts on page 4 of the answer that Katoh discloses that "a single channel is processing both the channel data and pseudo channel data to produce a clock signal at a single output RCK." Further, the examiner asserts that both Katoh and AAPA are concerned with reading and writing data to a disk drive. Finally, the examiner concludes that given the two prior art teachings it would be obvious to apply the dual input to a single PLL teaching of Katoh to the AAPA "thereby providing a read/write clock output responsive to the data and wobble signal of AAPA because it would have provided the mechanism to speed up the processing of the data."

We disagree with the examiner's reasoning. An obviousness analysis commences with a review and consideration of all the pertinent evidence and arguments. "In reviewing the examiner's decision on appeal, the Board must necessarily weigh all of the evidence and argument." ***In re Oetiker***, 977 F.2d 1443,

1445, 24 USPQ2d 1443, 1444 (Fed. Cir. 1992). "[T]he Board must not only assure that the requisite findings are made, based on evidence of record, but must also explain the reasoning by which the findings are deemed to support the agency's conclusion." ***In re Lee***, 277 F.3d 1338, 1344, 61 USPQ2d 1430, 1434 (Fed. Cir. 2002). In addition, our reviewing court stated in ***In re Lee,*** 277 F.3d at 1343, 61 USPQ2d at 1433, that when making an obviousness rejection based on combination, "there must be some motivation, suggestion, or teaching of the desirability of making the specific combination that was made by applicant" (quoting ***In re Dance***, 160 F.3d 1339, 1343, 48 USPQ2d 1635, 1637 (Fed. Cir. 1998)).

Claim 1 includes the limitation of "the phased locked loop generating a read clock signal when the drive is reading data, and the phase locked loop generating a write clock signal when the drive is writing data." Thus, the scope of independent claim 1 is that one Phase Locked Loop (PLL) generates both the read and write clock.

We find that both the AAPA and Katoh, teach systems where the write clock is generated by a separate PLL than the read clock. See, for example, figures 1 and 3 of Katoh, read clock signal RCK is generated by "Channel PLL" and write clock signal WCK is generated by "Wobble PLL."[2] We concur with the examiner that Katoh teaches "Channel PLL," which generated clock RCK, has input from either one of two sources (see column 7, lines 30-24). However, we find that this teaching is limited to the read clock, RCK, as Katoh explicitly teaches that the write clock is generated by a separate PLL than the read clock. Thus, we do not find that Katoh suggests that the same PLL

[2] Katoh teaches an embodiment of figure 3, which uses only one clock, RCK, however this embodiment is described in column 13, line 46, for a read only device, and as such has no need for a write clock.

should be used to generate both a read clock and write clock. Accordingly, we will not sustain the rejection of claims 1 and 2 under 35 U.S.C. § 103 as being unpatentable over the AAPA in view of Katoh.

Conclusion

The decision of the examiner rejecting claims 1 and 2 under 35 U.S.C. § 103 is reversed.

REVERSED

MICHAEL R. FLEMING Administrative Patent Judge	)	
JOSEPH L. DIXON Administrative Patent Judge	)	BOARD OF PATENT APPEALS AND INTERFRENCES
ROBERT E. NAPPI Administrative Patent Judge	)	

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